WAFER LEVEL CHIP SCALE PACKAGE

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ABSTRACT OF THE DISCLOSURE

A wafer level fabricated integrated circuit package having an air gap formed between the integrated circuit die of the package and a flexible circuit film located over and conductively attached to the die though raised interconnects formed on the die is described. The flexible circuit film further includes routing conductors that connect inner landings on the bottom surface of the flexible circuit film with outer landings on the top surface of the flexible circuit film. The outer landings are offset a horizontal distance from the inner landings. In some embodiments, contact bumps are formed on the outer landings of the flexible circuit film layer for use in connecting the package to other substrates. The wafer level chip scale package provides a highly compliant connection between the die and any other substrate that the die is attached to.